IN THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Presented) An integrated circuit, comprising:

a semiconductor die including at least one pair of bond pads and an input/output (I/O) bond pad, each pair of bond pads having a single corresponding bond wire connected thereto such that each bond pad of each of the at least one pair of bond pads has only one bond wire end connected thereto, a first bond pad of the at least one pair of bond pads located in an internal portion of the semiconductor die, the I/O bond pad to receive an I/O bond wire operable for electrically connecting to a package.

2. (Original) The integrated circuit of Claim 1 wherein the at least one pair of bond pads includes a second bond pad located along a periphery of the semiconductor die.

3. (Original) The integrated circuit of Claim 1 wherein the single corresponding bond wire comprises a metallic material selected from the group consisting of gold, aluminum, and copper.

4. (Original) The integrated circuit of Claim 1 wherein the single corresponding bond wire is bonded to the pair of bond pads using a wire bond type selected from the group consisting of ball bonds, stitch bonds, stitch bonds on bonding pad, and stitch bonds on ball.

5. (Previously Presented) The integrated circuit of Claim 1 further comprising a first trace in the semiconductor die connected between the pair of bond pads.

6. (Previously Presented) The integrated circuit of Claim 1 wherein the at least one pair of bond pads includes a second bond pad located in a non-internal portion of the semiconductor die.

7. (Original) The integrated circuit of Claim 1 wherein the single corresponding bond wire is selected from the group consisting of power interconnects, ground interconnects, and signal interconnects.

8. (Original) The integrated circuit of Claim 1 further comprising a plurality of pairs of bond pads, each of the pairs of bond pads having a corresponding wire connected therebetween such that each bond pad of the pairs of bond pads includes a single wire bond.

9. (Previously Presented) An integrated circuit, comprising:

a semiconductor die including at least one pair of electrical termination means and an input/output (I/O) electrical termination means, each pair of electrical termination means having a single corresponding means for conducting connected thereto such that each electrical termination means of the pair of electrical termination means has only one end of any means for conducting connected thereto, a first electrical termination means of each of the at least one pair of electrical termination means located in an internal portion of the semiconductor die, the I/O electrical termination means to receive an I/O means for conducting operable for electrically connecting to a package.

10. (Original) The integrated circuit of Claim 9 wherein the at least one pair of electrical termination means includes a second electrical termination means located along a periphery of the semiconductor die.

11. (Original) The integrated circuit of Claim 9 wherein the single corresponding means for conducting comprises a metallic material selected from the group consisting of gold, aluminum, and copper.

12. (Original) The integrated circuit of Claim 9 wherein the single corresponding means for conducting is bonded to the pair of electrical termination means using a wire bond type selected from the group consisting of ball bonds, stitch bonds, stitch bonds on bonding pad, and stitch bonds on ball.

13. (Previously Presented) The integrated circuit of Claim 9 further comprising a first trace in the semiconductor die connected between the pair of electrical termination means.

14. (Previously Presented) The integrated circuit of Claim 9 wherein the at least one pair of electrical termination means includes a second electrical termination means located in a non-internal portion of the semiconductor die.

15. (Original) The integrated circuit of Claim 9 wherein the single corresponding means for conducting is selected from the group consisting of power interconnects, ground interconnects, and signal interconnects.

16. (Original) The integrated circuit of Claim 9 further comprising a plurality of pairs of electrical termination means, each of the pairs of electrical termination means having a corresponding means for conducting connected therebetween such that each electrical termination means of the pairs of electrical termination means includes a single wire bond.

17-24. (Cancelled)

25. (Previously Presented) The integrated circuit of Claim 1 further comprising a second trace in the semiconductor die connected between the I/O bond pad and one of the pair of bond pads.

26. (Previously Presented) The integrated circuit of Claim 1 included in the package, the package including a lead finger; and

the I/O bond wire to connect between the I/O bond pad and the lead finger.

27. (Previously Presented) The integrated circuit of Claim 9 further comprising a second trace in the semiconductor die connected between the I/O electrical termination means and one of the pair of electrical termination means.

28. (Previously Presented) The integrated circuit of Claim 9 included in the package, the package including a means for connecting; and

the I/O conducting means to connect between the I/O electrical termination means and the connecting means.

29. (Previously Presented) An integrated circuit, comprising:

a semiconductor die including at least one pair of bond pads, a first bond pad of the at least one pair of bond pads located in an internal portion of the semiconductor die and having a first end of a first bond wire connected thereto, the first bond pad having only one bond wire connected thereto, a second bond pad of the at least one pair of bond pads located in a periphery of the semiconductor die and having a first portion and a second portion, the first portion of the second bond pad having a second end of the first bond wire connected thereto, the second portion of the second bond pad to receive an I/O bond wire for electrically connecting to leads of a package, wherein the leads are spaced from a periphery of the semiconductor die.

30. (Previously Presented) The integrated circuit of Claim 29 wherein the first bond wire comprises a metallic material selected from the group consisting of gold, aluminum, and copper.

31. (Previously Presented) The integrated circuit of Claim 29 wherein the first bond wire is bonded to the pair of bond pads using a wire bond type selected from the group consisting of ball bonds, stitch bonds, stitch bonds on bonding pad, and stitch bonds on ball.

32. (Previously Presented) The integrated circuit of Claim 29 further comprising a first trace in the semiconductor die connected between the pair of bond pads.

33. (Previously Presented) The integrated circuit of Claim 29 wherein the first bond wire is selected from the group consisting of power interconnects, ground interconnects, and signal interconnects.

34. (Previously Presented) The integrated circuit of Claim 29 further comprising a plurality of pairs of bond pads, each of the pairs of bond pads having a corresponding wire connected therebetween.

35. (Previously Presented) An integrated circuit, comprising:

a semiconductor die including at least one pair of electrical termination means, a first electrical termination means of the at least one pair of electrical termination means located in an internal portion of the semiconductor die and having a first end of a first means for conducting connected thereto, the first electrical termination means having only one conducting means connected thereto, a second electrical termination means of the at least one pair of electrical termination means located in a periphery of the semiconductor die and having a first portion and a second portion, the first portion of the second electrical termination means having a second end of the first conducting means connected thereto, the second portion of the second electrical termination means to receive an I/O conducting means for electrically connecting to leads of a package, wherein the leads are spaced from a periphery of the semiconductor die.

36. (Previously Presented) The integrated circuit of Claim 35 wherein the first conducting means comprises a metallic material selected from the group consisting of gold, aluminum, and copper.

37. (Previously Presented) The integrated circuit of Claim 35 wherein the first conducting means for conducting is bonded to the pair of electrical termination means using a wire bond type selected from the group consisting of ball bonds, stitch bonds, stitch bonds on bonding pad, and stitch bonds on ball.

38. (Previously Presented) The integrated circuit of Claim 35 further comprising a first trace in the semiconductor die connected between the pair of electrical termination means.

39. (Previously Presented) The integrated circuit of Claim 35 wherein the first conducting means is selected from the group consisting of power interconnects, ground interconnects, and signal interconnects.

40. (Previously Presented) The integrated circuit of Claim 35 further comprising a plurality of pairs of electrical termination means, each of the pairs of electrical termination means having a corresponding means for conducting connected therebetween.

41. (New) The integrated circuit of Claim 5, further comprising a second trace in the semiconductor die connected between the I/O bond pad and one of the pair of bond pads.

42. (New) The integrated circuit of Claim 13, further comprising a second trace in the semiconductor die connected between the I/O electrical termination means and one of the pair of electrical termination means.

43. (New) The integrated circuit of Claim 1, wherein the I/O bond pad and one of the pair of bond pads are arranged on a common bonding surface.

44. (New) The integrated circuit of Claim 9, wherein the I/O electrical termination means and one of the pair of electrical termination means are arranged on a common bonding surface.

45. (New) The integrated circuit of claim 29, further comprising a trace in the semiconductor die connected between the first portion and second portion of the second bond pad.

46. (New) The integrated circuit of claim 32, further comprising a second trace in the semiconductor die connected between the first portion and second portion of the second bond pad.

47. (New) The integrated circuit of claim 29, wherein the first portion and second portion of the second bond pad are arranged on a common bonding surface.

48. (New) The integrated circuit of claim 35, further comprising a trace in the semiconductor die connected between the first portion and second portion of the second electrical termination means.

49. (New) The integrated circuit of claim 38, further comprising a second trace in the semiconductor die connected between the first portion and second portion of the second electrical termination means.

50. (New) The integrated circuit of claim 35, wherein the first portion and second portion of the second electrical termination means are arranged on a common bonding surface.